M.C.A. DEGREE EXAMINATION, FEBRUARY 2012.
First Semester
DMC 1911 — COMPUTER ORGANIZATION
(Regulation 2009)
Time : Three hours
Maximum : 100 marks
Answer ALL questions.

PART A — (10 × 2 = 20 marks)
1. Convert the hexadecimal number 68BE to binary and then from binary, convert it to octal.
2. Simplify $xyz + x'y + xyz'$ to a minimum number of literals.
3. State the functionality of a Decoder.
4. What is a counter?
5. List the four phases of Instruction cycle.
7. What is the need for an interface between I/O device and the CPU?
8. Compare Synchronous with Asynchronous transfer modes.
9. Why the size of Cache and Main memory are related?
10. What is a control word?

PART B — (5 × 16 = 80 marks)
11. (a) (i) Simplify $F(w,x,y,z) = \sum (0,2,5,6,7,8,10)$ in Product of Sums. (8)

(ii) Draw a NAND logic diagram that implements the complement of the following function $F(A,B,C,D) = \sum (0,1,2,3,4,8,9,12)$. (8)

Or

(b) (i) Discuss the operation of full adder with circuit diagram and truth table. (8)

(ii) Explain the operation of JK flip flop with logic diagram, truth table and symbol. (8)
12. (a) (i) Implement the 4-input function
\[ F(A,B,C,D) = \sum (1,3,4,11,12,13,14,15) \] with a multiplexer. 
(ii) Design a serial adder circuit using shift registers and a full adder.

Or

(b) Design a 4-bit Up-Down binary counter circuit and explain its operation with state table.

13. (a) (i) State the need for Interrupts. Explain in detail about how it helps in I/O.
(ii) Explain subroutine with example.

Or

(b) Discuss various arithmetic and logic operations in detail.

14. (a) (i) Compare Isolated and Memory-Mapped I/O.
(ii) Discuss Asynchronous data transfer in detail.

Or

(b) Discuss in detail about DMA Controller and its functionality.

15. (a) Discuss various mapping procedures of Cache memory in detail.

Or

(b) (i) Write a note on register organization.
(ii) Explain various types of addressing modes.
1. Convert the following numbers to the bases indicated:
   (a) 7256 to octal
   (b) 175 to binary

2. Give the truth table for Full-Adder.

3. What is a multiplexer?

4. What are the steps involved in transferring a stored word out of memory?

5. Mention the purposes of program counter and accumulator.

6. Specify the names of the four tables used by an assembler.

7. Define peripheral. What are the three types of peripherals?

8. What is the purpose of data link protocol?

9. What is associative memory? Why is it so called?

10. Evaluate the arithmetic statement $X = (A + B) \times (C + D)$ using three-address instructions.
PART B — (5 × 16 = 80 marks)

11. (a) (i) Obtain the 1's and 2's complements of the following eight digit binary numbers: 10101110; 10000000, 00000000 and 11111111. (6)

(ii) What is a flip-flop? Explain the common types of flip-flops. (10)

Or

(b) (i) Perform the arithmetic operations (+70) + (+80) and (−70)+(−80) in binary using signed 2’s complement representation for negative numbers. (6)

(ii) Discuss full adder with logic diagram, characteristic table and derive its Boolean function. (10)

12. (a) What is a microoperation? Explain in detail the four categories of microoperations? (16)

Or

(b) (i) What is a bus? A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers. (8)

1) How many selection inputs are there in each multiplexer?

2) What size of multiplexers are needed?

3) How many multiplexers are there in the bus?

(ii) Explain the operation of a 4-bit binary counter with a neat diagram. (8)

13. (a) (i) What is an interrupt? Explain the steps to be carried out while serving an interrupt. (8)

(ii) Discuss subroutine with example. (8)

Or

(b) Explain in detail the two-pass assembler. (16)

14. (a) Discuss Direct Memory Access (DMA) in detail. (16)

Or

(b) Write notes on the following: (5+5+6)

(i) CPU-IOP Communication

(ii) Bit-oriented Protocol

(iii) Daisy-chaining priority.

15. (a) Explain in detail the three cache mapping techniques. (16)

Or

(b) Discuss various addressing modes in detail. (16)
Question Paper Code : 85702

M.C.A. DEGREE EXAMINATION, FEBRUARY 2011.

First Semester

DMC 1601 — COMPUTER ORGANIZATION

(Regulation 2007)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)


2. Distinguish between combinational circuit and sequential circuit.

3. Construct the truth table for 3 input NAND gate.

4. Represent the following conditional control statement by two register transfer statements with control functions.
   If \((P = 1)\) then \((R1 \leftarrow R2)\) else if \((Q = 1)\) then \((R1 \leftarrow R3)\)

5. Give the micro operation for the fetch and decode phases of the instruction cycle.

6. When is an instruction set said to be complete?

7. Compare isolated I/O and memory mapped I/O.

8. Define baud rate.

9. What is content addressable memory?

10. List out all the shift instructions.
11. (a) (i) What are the various methods used to represent the signed numbers in computer memory? Explain. (10)

(ii) Discuss the different binary codes with examples. (6)

Or

(b) Simplify the following Boolean function in sum-of-products form by means of a four variable map. Draw the logic diagram with

(i) NAND-OR gates

(ii) NAND gate.

\[ F(A, B, C, D) = \sum(0, 2, 8, 9, 10, 11, 14, 15) \] (16)

12. (a) (i) Draw a block diagram for 4-bit bidirectional shift register with parallel load and explain the operation. (10)

(ii) Explain the function of 3-to-8 decoder. (6)

Or

(b) Construct and explain the operation of 4-bit composite arithmetic circuit and discuss the arithmetic micro operations with examples. (16)

13. (a) Explain the various memory-reference instructions and the micro-operations needed for the execution of various memory reference instructions. (16)

Or

(b) Draw the flow chart and explain the operation of two-pass assembler. (16)

14. (a) Discuss the following:

(i) Daisy chaining priority interrupt. (8)

(ii) Input Output Processor (IOP). (8)

Or

(b) What are the different types of data transfer to and from peripherals? Explain each of them and write the advantages and disadvantages of each method. (16)
15. (a) What is virtual memory? Explain with a diagram how virtual address can be mapped into physical address using paging. (16)

Or

(b) (i) What are the types of addressing modes? Explain with examples. (10)

(ii) Write a note on program control instructions. (6)
PART A — (10 × 2 = 20 marks)

1. Differentiate combinational and sequential circuits.

2. Simplify the Boolean function, \( F(x, y, z) = \sum (1, 2, 3, 6, 7) \) using three variable maps.

3. The content of a 4-bit register is initially 1101. The register is shifted four times to the right with the serial input being 1011. What is the content of the register after each shift?

4. A 3-line-to-8 line decoder can be used for octal -to-decimal decoding. When a 1012 is on the inputs, which output line is activated?

5. What is the difference between a direct and indirect address instruction? How many references to memory are needed for each type of instruction to bring an operand to the processor register?

6. What is an assembler?

7. List out the advantages of using IOP.

8. What are the advantages of DMA transfer over interrupt driven data transfer?
9. What is the use of associative memory?

10. Differentiate Virtual memory from Cache memory.

PART B — (5 x 16 = 80 marks)

11. (a) (i) Simplify the Boolean function : \( \sum (0,1,2,4,5,6,8,9,12,13,14) \) using Map method. (10)

(ii) Implement the resulting function with NAND gates. (6)

Or

(b) (i) Represent decimal number 8620 in BCD, excess-3 code, 8421 code and as a binary number. (9)

(ii) Perform the arithmetic operation \((+42) - (-13)\) and \((-42) - (13)\) in binary using signed 2's complement representation for negative numbers. (7)

12. (a) (i) With the help of a neat sketch explain 4 to 1 multiplexer. (8)

(ii) Prove the universal property of the NAND gate. (8)

Or

(b) Write a note on:

(i) Register transfer language (10)

(ii) Tri state buffer. (6)

13. (a) (i) Draw the Timing diagram for a Instruction cycle and explain. (10)

(ii) Give a note on Subroutine. (6)

Or

(b) Explain the operation of a 2 – pass assembler with a neat flow chart. (16)

14. (a) (i) How is asynchronous transfer different from synchronous transfer? (4)

(ii) List the various sequence of control during an asynchronous transfer and explain with timing diagram. (12)

Or

(b) (i) What are the needs for an I/O interface? Discuss. (8)

(ii) Explain the operation of IOP with an example. (8)
15. (a) (i)  Draw one cell of associative memory and explain the matching logic.  

(ii)  Explain the terms: spatial locality and temporal locality.

Or

(b)  Write detailed account of the various addressing modes with examples.
First Semester
MC 1601 — COMPUTER ORGANIZATION
(Regulation 2006)

Time: Three hours

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Simplify the Boolean expression, if possible $A + AB + ABC$.

2. Convert the following decimal numbers to binary and add using the 2's complement form: $-110$ and $-84$.

3. How can a decoder be used as a multiplexer?

4. When is the following register transfer statement possible?

   $T : R2 ← R1, R1 ← R2$;

5. List the micro-operations for fetch and decode phase of basic computer.

6. An output program resides in memory starting from address 2300. It is executed after the computer recognizes an interrupt when FGO becomes a1. What must be the last two instructions of the output program?

7. What is the difference between isolated I/O and memory-mapped I/O?

8. What is the basic advantage of using interrupt initiated data transfer over transfer under program controlled with out an interrupt?

9. How many $128 \times 8$ RAM chips are needed to provide a memory capacity of 2048 bytes?

10. What is locality of reference?
PART B — (5 x 16 = 80 marks)

11. (a) (i) Use Karnaugh map to minimize the following SOP expression:

\[ BC\overline{D} + \overline{A}BC\overline{D} + \overline{A}BCD + \overline{A}B\overline{C}D + \overline{A}BCD + \overline{A}B\overline{C}D + \overline{A}BCD + \overline{A}BCD \]

\[ A\overline{BCD} + \overline{A}BCD \] (8)

(ii) Draw the circuit for full adder from the truth table using K-map. (8)

Or

(b) Design a 2-bit count-down counter. (16)

12. (a) (i) Construct a 16 to 1 line multiplexer with 2 8 to 1 line multiplexers and explain its operation by means of a function table. (10)

(ii) Show the block diagram of the hardware that implements the following register transfer statement \( P : R2 \leftarrow R1 \) (6)

Or

(b) (i) Given a 64 \times 8 ROM chip with the enable input, show the external connections necessary to construct a 256 \times 8 ROM with four chips and a decoder. (10)

(ii) Draw the block diagram of 4-bit synchronous binary counter and explain its operation. (6)

13. (a) (i) A computer uses a memory unit with 250 k words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.

(1) How many bits are there in the operation code, register code part and the address part?

(2) Draw the instruction word format and indicate the number of bits in each part?

(3) How many bits are there in the data and address inputs of memory? (3 \times 2 = 6)
(ii) Write an assembly program to multiply two positive numbers by repeated addition method. (10)

Or

(b) (i) How are interrupts handled by the basic computer? Explain the interrupt cycle with a flow chart. (10)

(ii) Write a sub routine to complement each word in a block of data. The subroutine takes two parameters: the starting address and the number of words in each block. (6)

14. (a) (i) What are interface units? Why are they needed? (6)

(ii) Explain the Daisy chain method of establishing priority. (10)

Or

(b) Explain the operation of serial communication processor with necessary protocols. (16)

15. (a) (i) Explain the mapping procedure for converting virtual address to physical address with necessary tables. (10)

(ii) What is page fault? How is it handled? (3 + 3)

Or

(b) (i) Explain the various instruction types based on the length. (6)

(ii) Write a note on the various addressing modes. (10)
M.C.A. DEGREE EXAMINATION, FEBRUARY 2008.

First Semester

DMC 1601 — COMPUTER ORGANIZATION

(Regulation 2007)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Simplify the following expression in sum of products and product of sum form:
   \[ xz' + y'z' + yz' + xy \]

2. A sequential circuit has 2D flip-flops A and B, two inputs x and y and one output z. The flip-flop input equations and the circuit output is as follows:
   \[ \begin{align*}
   D_A &= x'y + xA \\
   D_B &= x'B + xA \\
   z &= B
   \end{align*} \]

   Draw the logic diagram of the circuit.

3. Define the role of (a) Decoder (b) Multiplexer.

4. An 8-bit register contains the binary value 100111000. What is the register value after arithmetic shift right?

5. What are the instructions needed in the basic computer in order to set the K flip-flop?

6. How hardware and software interrupts are handled in a Computer System?

7. What is the difference between isolated I/O and memory mapped I/O?
8. What is the difference between synchronous and asynchronous transfer?

9. What is the use of virtual memory?

10. What are the advantages of microprogrammed control unit?

PART B — (5 x 16 = 80 marks)

11. (a) (i) What is the difference between a sequential and combinational circuit? (4)

(ii) Design a 3 bit counter that must go through the sequence as follows:

    0, 1, 3, 4, 6, 7, 0

Or

(b) (i) Draw the circuit diagram for full adder circuit and give its truth table. (6)

(ii) Construct a 4-bit adder circuit using full adders. (10)

12. (a) Construct a 3 to 8 line decoder with four 3 to 8 line decoder with enable and one 2 to 4 line decoder. (16)

Or

(b) Draw the block diagram for a 4-bit bi-directional shift register with parallel load. (16)

13. (a) (i) How registers inside the system are organized and how they access the shared bus for computation. (8)

(ii) Write notes on:

(1) Instruction cycle. (4)

(2) I/O and interrupt. (4)

Or

(b) Write a subroutine for basic computer to subtract two numbers. In the calling program BSA instruction must be followed with subtrahend and minuend. The function should return the answer in the very next location. (16)

14. (a) (i) Explain the various ways of implementing priority interrupt. (10)

(ii) Explain the interrupt cycle. (6)

Or

(b) Explain the operation of I/O processor. (16)
15. (a) (i) What is locality of reference? (4)
(ii) Explain the mapping procedures used in cache memory. (12)

Or

(b) (i) What is the need for addressing modes? Explain few with their syntactical behaviour. (8)
(ii) Explain briefly about paging and segmentation concepts in memory organisation. (8)
M.C.A. DEGREE EXAMINATION, FEBRUARY 2009.

First Semester

DMC 1601 — COMPUTER ORGANIZATION

(Regulation 2007)

Time: Three hours

Maximum: 100 marks

Answer ALL questions.

PART A — (10 x 2 = 20 marks)

1. Convert (736.4)8 to decimal number.

2. Give the Algebraic function and the truth table for the “AND” gate.

3. Define Multiplexer with an example.

4. A 8 bit register contains the binary value 01011100. What is the register value after arithmetic shift right? What is it value after a logical shift right?

5. What is the differences between a direct and an indirect address instruction?

6. Mention the purpose of the fields in every line of assembly language program.

7. Define the term peripherals. Mention the types of peripherals.

8. What are the modes of data transmission between two points?

9. Define Associative memory and virtual memory.

10. What is the use of control word?
PART B — (5 × 16 = 80 marks)

11. (a) (i) Perform the arithmetic operations \((+42) + (-13)\) and \((-42)-(-13)\) in binary using signed-2's complement representation for negative numbers. \((6\) marks\)

(ii) Design a 2-bit binary counter with two JK flip-flops and one input \(x\). When \(x=0\), the state of the flip-flops does not change. When \(x=1\), the state sequence is 00, 01, 10, 11, 00 and repeat. \((10\) marks\)

Or

(b) (i) Represent the decimal number 8620 in

1. BCD
2. Excess-3 code
3. 2421 code
4. As a binary number. \((4\times2=8\) marks\)

(ii) Derive the truth table for full-adder and draw the circuit diagram. \((8\) marks\)

12. (a) (i) What is a decoder? Construct 2-to-4 line decoder with NAND gates. Explain its operation with the truth table. \((8\) marks\)

(ii) Draw the diagram of a 4-bit adder-subtractor and explain its operation. \((8\) marks\)

Or

(b) (i) What is bus? A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

1. How many selection inputs are there in each multiplexer?
2. What size of multiplexers are needed?
3. How many multiplexers are there in the bus? \((8\) marks\)

(ii) The 8 bit registers AR, BR, CR, and DR initially has the following values:

\[
\begin{align*}
AR &= 11110010 \\
BR &= 11111111 \\
CR &= 10111001 \\
DR &= 11101010
\end{align*}
\]

Determine the 8 bit values in each register after the execution of the following sequence of micro operations.

\[
\begin{align*}
AR &\leftarrow AR + BR \text{ to } AR \\
CR &\leftarrow CR \land DR, \text{ BR }\leftarrow BR + 1 \text{ And } DR \text{ to } CR, \text{ increment } BR \\
AR &\leftarrow AR - CR \text{ Subtract CR from AR.}
\end{align*}
\]

\((8\) marks\)
13. (a) A computer uses a memory unit with 256 K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part.

(i) How many bits are there in the operation code, the register code part and the address part?

(ii) Draw the instruction word format and indicate the number of bits in each part.

(iii) How many bits are there in the data and address inputs of the memory? \(16\)

Or

(b) (i) List the various registers of a basic computer and specify the purpose of each register. \(8\)

(ii) What are the three basic computer instructions? Give the format of each. Mention any two examples for each. \(8\)

14. (a) (i) Explain the different modes of data transfer to and from peripherals. \(10\)

(ii) What is the purpose of an Input-Output interface? What are the major differences between the computer and a peripheral? \(6\)

Or

(b) Explain the following:

(i) First-in, First-out buffer.

(ii) Daisy-chaining priority.

(iii) CPU-IOP communication. \(5 + 5 + 6\)

15. (a) Explain the basic operation of the cache memory. Explain various types of mapping procedures related to the cache memory organization. \(16\)

Or

(b) Draw the instruction format with mode field. Discuss in detail about various addressing modes. An instruction is stored at location 300 with its address field at location 300 with its address at location 301. The address field has the value 400. A processor register R 1 contains the number 200.
Evaluate the effective address if the addressing mode of the instruction is

(i) Direct
(ii) Immediate
(iii) Relative
(iv) Register indirect
(v) Index with R 1 as the index register.  

(16)